

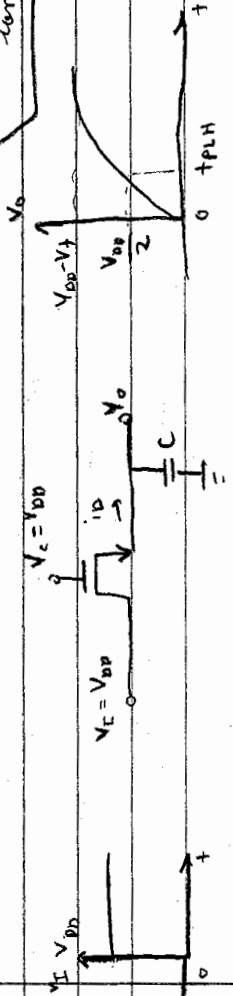
Pass Transistor Logic (PTL)

* every circuit node has at all times a low resistance path to V_{DD} or ground.

body effect: $V_t = V_{t0} + \gamma (\sqrt{V_{SB} + 2\phi_f} - \sqrt{2\phi_f})$

$|V_{tp}| = V_{tp0} + \gamma (\sqrt{V_{BS} + 2\phi_f} - \sqrt{2\phi_f})$

connect PMOS to V_{DD}
connect NMOS to ground



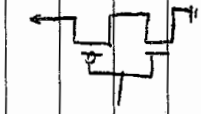
* as V_t goes high,

transistor saturation

mode $i_D = \frac{1}{2} k_n (V_{DD} - V_o - V_t)^2$

$k_n = K_n' (W/L)$

$V_t = V_{t0} + \gamma (\sqrt{V_o + 2\phi_f} - \sqrt{2\phi_f})$



① "poor" connected to V_{DD} input to inverter can cause inverter conduction (power dissipation)

② at $t=0$, $V_t = V_{t0}$ and i_D large.

as C charges and V_o rises, V_t increases

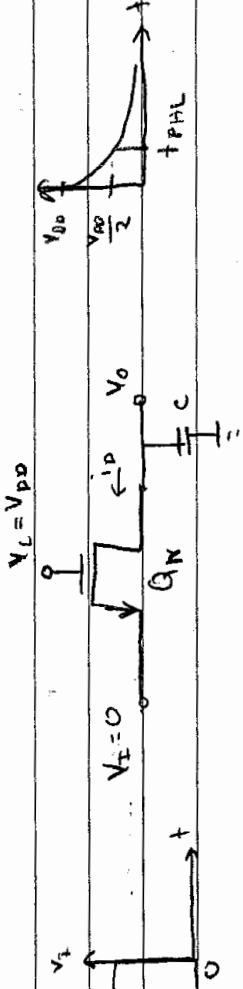
and i_D decreases. (slow charging)

③ i_D reduces to zero when $V_o = V_{DD} - V_t$

$\therefore V_{OH} = V_{DD} - V_t$

R can be $(2V_{t0})$.

④ t_{PLH} is time for V_o reach $V_{DD}/2$



note another cause? drain

$V_p > V_s$

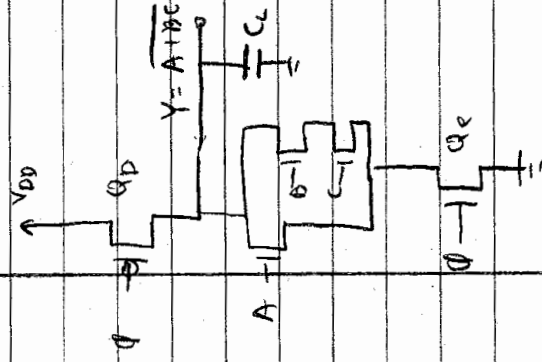
⑤ as V_t drops down to 0V.

$V_o = V_{DD}$ and saturation region: $i_D = \frac{1}{2} k_n (V_{DD} - V_t)^2$

no body effect, $V_t = V_{t0}$, as C discharges V_o decreases and

Q_N enters triode region at $V_o = V_{DD} - V_t$. Full discharge to $V_{oL} = 0$ "good" mos

Dynamic Logic Circuits



pre-charge phase (Q is low) $\rightarrow Q_p$ on
 evaluation phase (Q is high) $\rightarrow Q_p$ off and Q_n on

C_L = capacitance between output and ground.

$\rightarrow Q_p$ charges C_L so $V_{DD} = V_Y$ after pre-charge

A, B, C change and while being pre-charge.

\rightarrow evaluation \Rightarrow if Y high after logic PDN no conduct

output remains V_{DD} and $t_{PHL} = 0, V_Y = V_{DD}$

if Y low after logic, PDN conducts

through Q_n and C_L discharge through PDN,

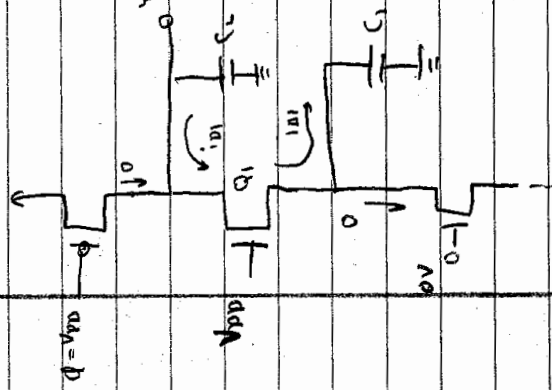
$\hookrightarrow Q_n$ adds to t_{PHL} $V_Y = 0$

Non-ideal effects ① leakage of C_L due to slow discharge over time

② Charge sharing \rightarrow beginning of evaluation phase

after Q_p off and with C_L charged to V_{DD}

Q_1 has high and Q_2 low.

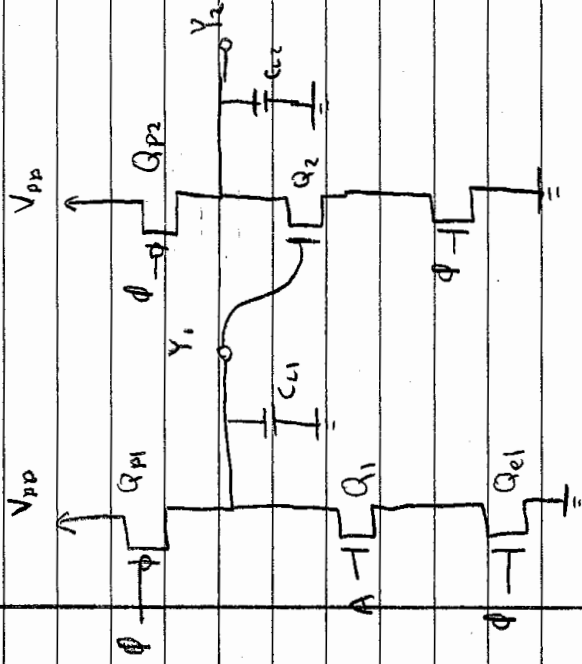


① pre-charge C_L

add to capacitance

② charge C_L

Cascading Dynamic Logic



Pre-charge phase C_{L1} and C_{L2}

will be charged through Q_{p1} and Q_{p2}

At end of pre-charge,

$$V_{Y1} = V_{DD} \text{ and } V_{Y2} = V_{DD}$$

Evaluation phase begins, for high A

$$(V_{Y1} = 0) \quad (V_{Y2} = V_{DD})$$

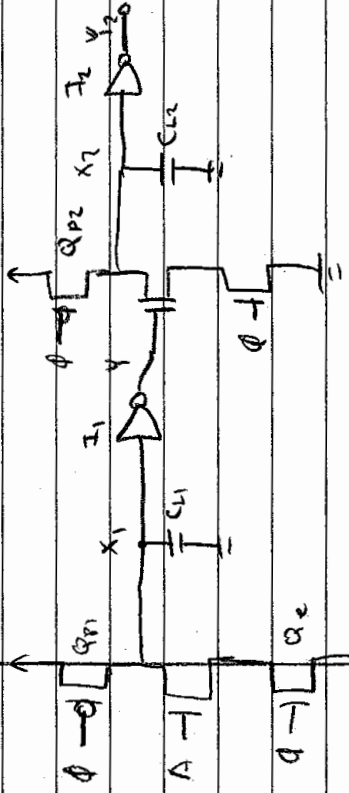
→ should get Y_1 low and Y_2 high.

Q_1 turns on and C_{L1} begins discharge

Q_2 turns on and C_{L2} also discharges

When V_{Y1} drops below V_{th} , Q_2 turns off; but by that time C_{L2} least charge and V_{Y2} less than V_{DD} expected.

Design Dynamic CMOS Logic:



pre-charge $\Rightarrow X_1$ and V_{DD} on output

Y_1 is at V_{DD} , X_2 at V_{DD}

and Y_2 is at V_{DD}

evaluation \Rightarrow (assume A high), ϕ high,

C_{L1} discharges and pulls X_1 down

Low input at Q_2 keeps Q_2 off and C_{L2} remains fully charged

1 domino gate

when V_{Y1} falls below threshold of Q_2 ,

Y_1 increases, turning Q_2 on and C_{L2}

begins discharging, pulls X_2 low. $\Rightarrow Y_2 \rightarrow V_{DD}$