

ECE/CS 252

FALL 2006

Professor Ramanathan

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Homework Assignment #5 SOLUTIONS

Due: Wed, Nov 8th at the beginning of class

1. Problem 4.5 [except for part b (3)]
 - (a) Location 3 contains 0000 0000 0000 0000
Location 6 contains 1111 1110 1101 0011
 - (b)
 - i. Two's Complement -
Location 0: 0001 1110 0100 0011 = 7747
Location 1: 1111 0000 0010 0101 = -4059
 - ii. ASCII - Location 4: 0000 0000 0110 0101 = 101 = 'e'
 - iv. Unsigned -
Location 0: 0001 1110 0100 0011 = 7747
Location 1: 1111 0000 0010 0101 = 61477
 - (c) Instruction - Location 0: 0001 1110 0100 0011 = Add R7 R1 R3
 - (d) Memory Address - Location 5: 0000 0000 0000 0110 Refers to location 6. Value stored in location 6 is 1111 1110 1101 0011
2. Problem 4.7
60 opcodes = 6 bits
32 registers = 5 bits
So number of bits required for IMM = 32 - 6 - 5 - 5 = 16
Since IMM is a 2's complement value, its range is $-2^{15} \dots (2^{15} - 1) = -32768 \dots 32767$.
3. Problem 4.8
 - a) 8-bits
 - b) 7-bits
 - c) Maximum number of unused bits = 3-bits
4. Problem 5.1
 - (a) ADD
 - operate
 - register addressing for destination and source 1
 - register or immediate addressing for source 2
 - (b) JMP
 - control
 - register addressing

- (c) LEA
 - data movement
 - immediate addressing
- (d) NOT
 - operate
 - register addressing

5. Problem 5.2

The MDR is 64 bits. The statement does not tell anything about the size of the MAR.

6. Problem 5.4

- (a) 8 bits
- (b) 6
- (c) 6

7. Problem 5.5

- (a) Addressing mode: mechanism for specifying where an operand is located.
- (b) An instruction's operands are located as an immediate value, in a register, or in memory.
- (c) The 5 are: immediate, register, direct memory address, indirect memory address, base + offset address. An immediate operand is located in the instruction. A register operand is located in a register (R0 - R7). A direct memory address, indirect memory address and base + offset address all refer to operands located in memory.
- (d) Add R2, R0, R1 => register addressing mode.

8. Problem 5.8

Increasing the number of registers to 32 will need 5 bits to denote the register number. Now, the minimum number of bits needed for the ADD instruction will be 4 (for the opcode) + 3 registers * 5 bits = 19 bits. This cannot fit in the 16-bits allocated for an lc-3 instruction.

9. Problem 5.9

- (a) Add R1, R1, #0 => differs from a NOP in that it sets the CC's.
- (b) BRnzp #1 => Unconditionally branches to one after the next address in the PC. Therefore no, this instruction is not the same as NOP.
- (c) Branch that is never taken. Yes same as NOP.